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10/720,614	11/24/2003	Martin G. Rammel	03-0945	4243
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HUGH P. GORTLER			EXAMINER	
23 Arivo Drive			DAO, THUY CHAN	
Mission Viejo, CA 92692				
			ART UNIT	PAPER NUMBER
			2192	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/720,614

Applicant(s)

RAMMEL, MARTIN G.

Examiner

THUY DAO

Art Unit

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 May 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17 and 31-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 17 and 31-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/06)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Paper No(s)/Mail Date _____
- 6) ☐ Other: _____

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on May 15, 2009 has been entered.

2. Claims 17 and 31-37 have been examined.

Response to Amendments

3. In the instant amendment, claims 17, 31, 32, and 35 have been amended.

4. The objection to claims 31, 32, and 35 is withdrawn in view of Applicant's amendments.

Response to Arguments

5. Applicants' arguments have been considered. After further consideration, the examiner notes that Ballagh (art of record, US Patent No. 6,883,147) still teaches the newly amended limitations.

a) The Applicants asserted, "Ballagh does not teach or suggest two separate chips: a CPU and FPGA. Ballagh discloses a single chip 202" (Remarks, page 4).

The examiner respectfully disagrees. Ballagh explicitly teaches:

a separate central processing unit (CPU) (e.g., FIG. 2, an "external processor" (a host CPU) coupled to bus-host interface 208, col.5: 22-28); *and*

a Field Programmable Gate Array (FPGA) (e.g., FIG. 2, chip 202, which is "an FPGA from Xilinx", col.5: 6-9).

b) The Applicants further asserted, "Ballagh is silent about dataflow between a CPU and an FPGA. Ballagh only discloses dataflow between the embedded processor 204 and the embedded peripheral 210." (Remarks, page 4).

The examiner respectfully disagrees. Ballagh explicitly teaches *dataflow between a CPU and an FPGA* (e.g., col.5: 22-28, communication between the external processor (the host CPU) and the peripheral component 210, which is embedded in chip/FPGA 202; col.5: 34-38, new coefficients are transferred from the external processor (the host CPU) to the processor 204, which is the embedded processor of the chip/FPGA 202).

c) The Applicants lastly asserted, "Ballagh does not teach or suggest running a first portion of a numerical simulation on a CPU and a second portion of a numerical simulation on an FPGA" (Remarks, pp. 405).

The examiner respectfully disagrees. Per the plain language of claims, Ballagh explicitly teaches:

using the CPU (e.g., FIG. 2, an "external processor" (host CPU) coupled to bus-host interface 208, col.5: 22-28)

to perform a numerical simulation including generating input signals (e.g., col.4: 47-64, the host CPU and a system-level simulation environment 110) *and*

a FPGA (e.g., FIG. 2, chip 202, which is "an FPGA from Xilinx", col.5: 6-9) *sending the input signals to the FPGA* (e.g., col.5: 28, from the external processor (host computer/CPU), transferring new filter coefficients to processor 204 (embedded within chip/FPGA 202));

using the FPGA to apply a model to the input signals (e.g., FIG. 2, col.5: 6-14, chip/FPGA 202 has peripheral component 210, which includes a reconfigurable digital filter to process the input signals, col.5: 19-22; FIG. 3A, col.5: 39-54, said reconfigurable digital filter has specific "control logic that manages coefficient reloading, adjusts data rates, and controls filter output frame buffering", i.e., applying a specific model to the input signals) *and send results of the model back to the CPU* (e.g., col.5: 29-34).

Claim Rejections – 35 USC §102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 31 is rejected under 35 U.S.C. 102(e) as being anticipated by Ballagh (art of record, US Patent No. 6,883,147).

Claim 31:

Ballagh discloses *a method of performing a numerical simulation with a Field Programmable Gate Array (FPGA) and a separate central processing unit (CPU), the method comprising:*

using the CPU (e.g., FIG. 2, an “external processor” (host CPU) coupled to bus-host interface 208, col.5: 22-28)

to perform a numerical simulation including generating input signals (e.g., col.4: 47-64, the host CPU and a system-level simulation environment 110) *and*

a FPGA (e.g., FIG. 2, chip 202, which is “an FPGA from Xilinx”, col.5: 6-9)

sending the input signals to the FPGA (e.g., col.5: 28, from the external processor (host computer/CPU), transferring new filter coefficients to processor 204 (embedded within chip/FPGA 202));

using the FPGA to apply a model to the input signals (e.g., FIG. 2, col.5: 6-14, chip/FPGA 202 has peripheral component 210, which includes a reconfigurable digital filter to process the input signals, col.5: 19-22; FIG. 3A, col.5: 39-54, said reconfigurable digital filter has specific “control logic that manages coefficient reloading, adjusts data rates, and controls filter output frame buffering”, i.e., applying a specific model to the input signals) *and send results of the model back to the CPU* (e.g., col.5: 29-34)

the FPGA also generating a first output that marks data as valid or invalid (e.g., FIG. 3A, FPGA 202 generating "coef_we" (first output) to mark "coef" valid or invalid and sending "coef_we" to its sub-component FIR filter 250, col.5: 55-65),
a second output that indicates the first sample of each frame (e.g., FIG. 3A, output port "yn" indicating data in output frames, col.5: 29-38 and 43-48), and
a third output that indicates when the model can accept data (e.g., FIG. 3A, FPGA 202 generating "rfd" indicating status "busy" or not, col.5: 55-65); and
wherein the CPU uses the results in the numerical simulation and the outputs to maintain data flow with the FPGA (e.g., col.6: 30-39, when the FIFO is full, initiating a filter reload sequence and issuing read requests to obtain new coefficients from the external processor, col.5: 34-38).

Claim Rejections – 35 USC §103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballagh in view of APA (art of record, Admitted Prior Art).

Claim 32:

Ballagh does not explicitly disclose *the method of claim 31, wherein the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT.*

However, in an analogous art, APA further discloses *the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 33:

Ballagh discloses *the method of claim 32, wherein the FPGA converts inputs from double point precision to fixed point prior to performing the transform* (e.g., col.3: 52-65; col.5: 29-38); *and wherein the FPGA converts the results from fixed point back to double precision prior to sending the results back to the CPU* (e.g., col.4: 65 – col.5: 38; col.6: 47-65).

APA further discloses *the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 34:

APA further discloses *the method of claim 32, wherein the CPU performs a numerical simulation of a radar system* (e.g., page 2: 4-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to as set forth above.

Claim 35:

Ballagh discloses *an apparatus* which recite(s) the same limitations as those of claim 31, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claim(s), it also teaches all of the limitations of claim 35.

APA further discloses *a numerical simulation of sine wave functions representing real and imaginary inputs; and performing an FFT on the inputs* (e.g., page 2: 4-23).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to transform a digitized waveform in the time domain into a digital representation in the frequency domain using Simulink simulation software as suggested by APA (e.g., page 2: 5-9 and 20-23).

Claim 36:

Ballagh discloses *the apparatus of claim 35, wherein the FPGA converts the real and imaginary inputs from double point precision to fixed point prior to performing the transform* (e.g., col.5: 1-38; col.6: 47-65); *and*

wherein the FPGA converts the results of the FFT from fixed point back to double precision prior to sending the results back to the CPU (e.g., col.3: 52-65; col.4: 65 – col.5: 38).

Claim 37:

APA further discloses *the apparatus of claim 35, wherein the CPU performs a numerical simulation of a radar system* (e.g., page 2: 4-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine APA's teaching into Ballagh's teaching. One would have been motivated to do so to as set forth above.

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ballagh in view of APA and US Patent Publication No. 2002/0103839 A1 to Ozawa (art made of record, hereafter "Ozawa").

Claim 17:

The rejection of claim 32 is incorporated. Ballagh discloses *coupling an output of a double delay block to a third input of the FFT block, the third input being adapted to mark data input as valid or invalid* (e.g., FIG. 3A, FPGA 202 generating "coef_we" (first output) to mark "coef" valid or invalid and sending "coef_we" to its sub-component FIR filter 250, col.5: 55-65).

APA further discloses *performing receiving the real and imaginary inputs at first and second inputs of an FFT block via a pair of gateway in blocks* (e.g., page 2: 4-23).

Neither Ballagh nor APA explicitly discloses other limitations. However, in an analogous art, Ozawa discloses:

coupling an output of a $k=0$ block to a fourth input of the FFT block (e.g., [0166] and [1203]),

the fourth input being adapted to control a forward or a reverse transform (e.g., [0351], performing cascade processing signals);

coupling outputs of FFT block to at least one D flip flop-based registers adapted to provide a signal latency; and coupling the outputs of the registers to at least one gateway out (e.g., [1268]-[1269]).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Ozawa's teaching into Ballagh and APA's teaching. One would have been motivated to do so to process data in an arithmetic device as suggested by Ozawa (e.g., [0007]-[0011]).

Conclusion

11. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570,

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respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Twee Dao/

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